Bidirectional Hybrid Switched-Inductor Switched-Capacitor Converter Topology with High Voltage Gain

Dan Hulea [1], Nicolae Muntean [1], Mihaita Gireada [1], Octavian Cornea [1], Emanuel Serban [2]
[1] Politehnica University of Timisoara [2] University of British Columbia
[1] Piata Victoriei No. 2 [2] 2332 Main Mall
[1] Timisoara, Romania [2] Vancouver, BC, Canada
Tel.: [1] +40-256-403-450 [2] +1 604-822-6024
E-Mail: dan.hulea@student.upt.ro; nicolae.muntean@upt.ro; mihaita.gireada@student.upt.ro; octavian.cornea@upt.ro; emanuel.serban@ieee.org
URL: [1] http://www.et.upt.ro/en [2] https://www.ubc.ca

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Keywords

« Converter circuit », « Converter control », « Wide input voltage range », « Supercapacitor », « High voltage power converters ».

Abstract

This paper proposes a new bidirectional hybrid DC-DC converter which uses a combination of a switched-capacitor and switched-inductor structure. The hybrid structure, based on the switched inductor and capacitor cells, helps achieve multiple advantages such as higher voltage conversion ratio, passive component size reduction, and active switch stress reduction. The mathematical analysis of the new converter is performed, addressing its control and stability through small-signal analysis modeling, and simulation results are used to confirm the theoretical considerations.

Introduction

Bidirectional converters are key elements in microgrid structures when used as an interface between the dc-bus and the storage element such as batteries and supercapacitors [1]–[3], and in hybrid storage systems consisting of the two storage elements [4]. Bidirectional converters are also commonly used in electric vehicles, either for vehicle to grid or regenerative braking system applications [5]–[7].

In applications with supercapacitor storage, in order to utilize the total storage capacity, it is necessary to operate on a wider voltage range and particularly at a lower voltage, therefore a high voltage conversion ratio converter is recommended. High voltage conversion ratio converters can use transformers or coupled inductors, quadratic structures [8], [9], parallel/series connected capacitors [10], [11], and hybrid structures with symmetrical switched capacitive or inductive cells [12]–[14].

Converter Topology and Analytical Descriptions

The proposed Bidirectional Hybrid Switched-Inductor Switched-Capacitor (Fig. 1 - BHSISC) has a hybrid structure comprised of two switched cells: a capacitive cell [13] and an inductive cell [14], [15], series connected. Even if the converter has four switching devices, its control is simple as only one signal is required to drive S_3/S_4 directly and inverted for S_2/S_1. The equivalent schematic for the two switching intervals t_{on} (t_{on} for buck operation) and t_{off} are presented in Fig. 2 and Fig. 3 respectively. The analysis is performed for the buck operation mode, where the only difference for the boost mode is the sign of the currents, as follows: $I_{L_1}, I_{L_2}, I_{L_3} > 0$ for buck mode; $I_{L_1}, I_{L_2}, I_{L_3} < 0$ for boost mode.

The switched-capacitive cell allows achieving a voltage doubling effect during t_{on} and a voltage halving during t_{off}, by connecting the switched-capacitors (C_1 & C_2) in series and in parallel. The switched-inductive cell (L_1 & L_2) allows a current doubling during t_{off} and a current halving during t_{on}, by connecting the inductors in series and then in parallel. On the higher voltage side (V_H), the insertion of the inductor L_3 leads to lower current ripple, in comparison to the conventional boost converter. Fig. 4 shows some key waveforms for the buck operation mode, the boost operation mode being very similar.

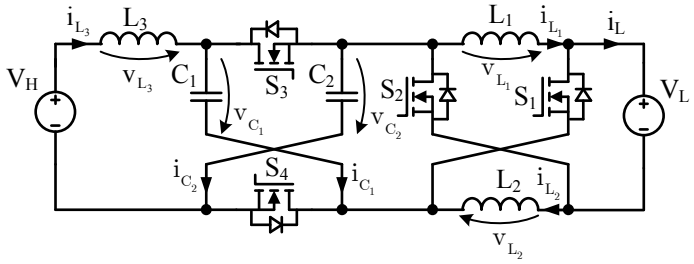

Fig. 1. Proposed Bidirectional Hybrid Switched-Inductor Switched-Capacitor (BHSISC) converter topology.

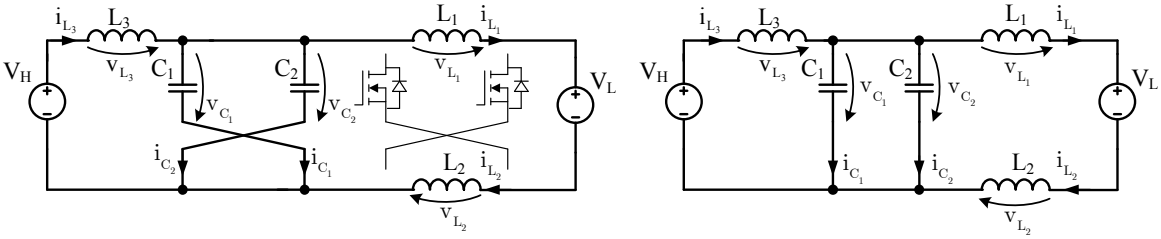

Fig. 2. BHSISC equivalent circuit during t_{on} (S_1, S_2 are switched off and S_3, S_4 are switched on).

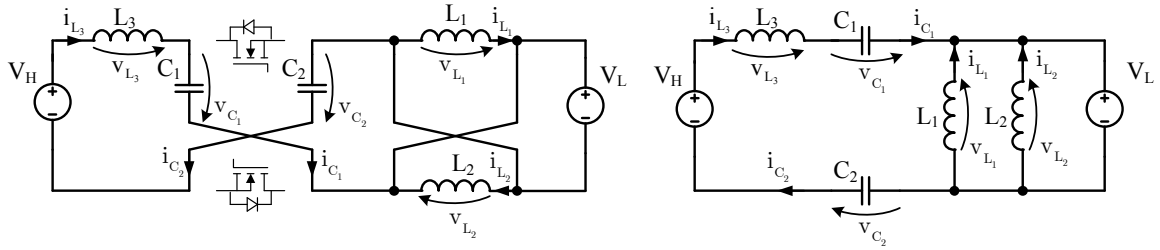

Fig. 3. BHSISC equivalent circuit during t_{off} (S_1, S_2 are switched on and S_3, S_4 are switched off).

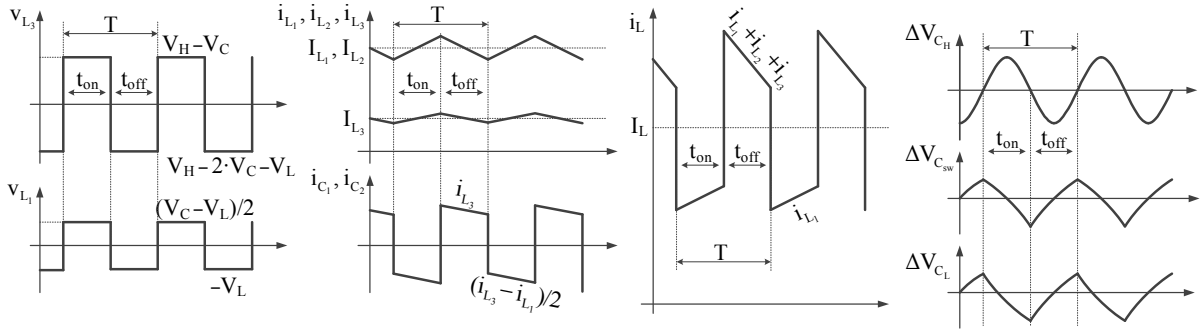

Fig. 4. Key waveforms of the proposed BHSISC converter.

The equations for the two switching states are derived in (1). In order to simplify the mathematical analysis, the following assumptions are made: the two switched inductors, L_1 and L_2 and their currents are equal; the two switched capacitors, C_1 and C_2, and their voltage are equal. Taking the assumption into consideration, the new simplified equations can be written as in (2).

$$t_{on}:\begin{cases} v_{L_3}=V_H-v_{C_1} \\ v_{L_1}+v_{L_2}=v_{C_1}-V_L \\ i_{C_1}+i_{C_2}=i_{L_3}-i_{L_1} \\ i_{L_1}=i_L \end{cases} \quad t_{off}:\begin{cases} v_{L_3}=V_H-v_{C_2}-V_L-v_{C_1} \\ v_{L_1}=v_{L_2}=-V_L \\ i_{C_1}=i_{C_2}=i_{L_3} \\ i_L=i_{C_1}+i_{L_1}+i_{L_2} \end{cases} \tag{1}$$

$$t_{on}:\begin{cases} v_{L_3}=V_H-v_{C_1} \\ v_{L_1}=(v_{C_1}-V_L)/2 \\ i_{C_1}=(i_{L_3}-i_{L_1})/2 \\ i_L=i_{L_1} \end{cases} \quad t_{off}:\begin{cases} v_{L_3}=V_H-2\cdot v_{C_1}-V_L \\ v_{L_1}=-V_L \\ i_{C_1}=i_{L_3} \\ i_L=i_{L_3}+2\cdot i_{L_1} \end{cases} \tag{2}$$

In order to obtain the voltage conversion ratio between V_H and V_L other assumptions are made: the capacitance value of C_1 and C_2 are sufficiently large to consider a constant voltage across their terminals and the circuit elements are considered ideal. With this hypothesis, and considering the duty cycle for the buck mode ($D=t_{on}/T$), the averaged inductor voltages in steady-state converter operation can be written as in (3), and the capacitor voltage is determined in (4).

$$\begin{cases} V_{L_3}=D\cdot(V_H-V_{C_1})+(1-D)\cdot(V_H-2V_{C_1}-V_L)=0 \\ V_{L_1}=D\cdot\dfrac{V_{C_1}-V_L}{2}+(1-D)\cdot(-V_L)=0 \end{cases} \tag{3}$$

$$\begin{cases} V_{C_1}=\dfrac{V_L\cdot(D-1)+V_H}{2-D} \\ V_{C_1}=V_L\cdot\dfrac{(2-D)}{D} \end{cases} \tag{4}$$

From (4) the relations between the low voltage (V_L), the high voltage (V_H), the duty cycle (D), and the switched capacitor (C_1) voltage can be written as in (5).

$$V_L=\frac{D}{4-3D}V_H;\quad D=\frac{4V_L}{V_H+3V_L};\quad V_{C_1}=\frac{V_H+V_L}{2}; \tag{5}$$

Converter Sizing

In order to test the proposed topology and further to compare it to other state-of-the-art topologies, a suitable selection of passive components must be made, therefore the calculation for the inductors and capacitors is presented in the following section.

Inductor sizing

The inductor value is selected from (6), and choosing an initial ripple percentage value for the inductor currents, defined in (7), the inductors are calculated as in (8). The inductor ripple percentage is considered at a certain level, so a fair comparison can be made with other topologies with respect to the inductor size.

$$t_{on}:\begin{cases} L_1\cdot\dfrac{di_{L_1}}{dt}=\dfrac{V_{C_1}-V_L}{2} \\ L_3\cdot\dfrac{di_{L_3}}{dt}=V_H-V_{C_1}\end{cases}\Rightarrow\begin{cases} L_1\cdot\dfrac{\Delta i_{L_1}}{t_{on}}=\dfrac{V_{C_1}-V_L}{2} \\ L_3\cdot\dfrac{\Delta i_{L_3}}{t_{on}}=V_H-V_{C_1}\end{cases}\Rightarrow\begin{cases} L_1=\dfrac{D\cdot T\cdot(V_{C_1}-V_L)}{2\cdot\Delta i_{L_1}} \\ L_3=\dfrac{D\cdot T\cdot(V_H-V_{C_1})}{\Delta i_{L_3}}\end{cases} \tag{6}$$

$$\begin{cases}\Delta i_{L1}=\Delta i_{Lp}\cdot I_{L1} \\ \Delta i_{L3}=\Delta i_{Lp}\cdot I_{L3}\end{cases} \tag{7}$$

$$\begin{cases} L_1=\dfrac{2\cdot V_L\cdot V_H\cdot(V_H-V_L)}{\Delta i_{Lp}\cdot f\cdot I_L\cdot({V_H}^2+4\cdot V_L\cdot V_H+3\cdot {V_L}^2)} \\ L_3=\dfrac{2\cdot V_H\cdot(V_H-V_L)}{\Delta i_{Lp}\cdot f\cdot I_L\cdot(V_H+3\cdot V_L)}\end{cases} \tag{8}$$

Capacitor sizing

The capacitor design is done similarly to the inductor design, by integrating the charge or discharge current over a specific time period as in (9) and choosing a desired voltage ripple for each capacitor as in (10). The voltage ripple is also chosen as a percentage of the capacitor voltage for the same reasons as for the inductor design. Taking this into consideration, the capacitor values are calculated as in (11).

$$\begin{cases} C_1\cdot\dfrac{dv_{C_1}}{dt}=\dfrac{i_{L_3}-i_{L_1}}{2} \\ C_L\cdot\dfrac{dv_{C_L}}{dt}=i_{L_1}-I_L \\ C_H\cdot\dfrac{dv_{CH}}{dt}=i_{L_3}-I_{L_3}\end{cases}\Rightarrow\begin{cases} C_1=\dfrac{1}{2\cdot(-\Delta v_{C_1})}\int_0^{t_{on}}(i_{L_3}-i_{L_1})dt \\ C_L=\dfrac{1}{(-\Delta v_{C_L})}\int_0^{t_{on}}(i_{L_1}-I_L)dt \\ C_H=\dfrac{1}{\Delta v_{C_H}}\int_{t_{on}/2}^{t_{on}+t_{off}/2}(i_{L_3}-I_{L_3})dt\end{cases} \tag{9}$$

$$\begin{cases}\Delta v_{C_1}=\Delta v_{Cp}\cdot V_{C_1} \\ \Delta v_{C_L}=\Delta v_{Cp}\cdot V_{C_L} \\ \Delta v_{C_H}=\Delta v_{Cp}\cdot V_{C_H}\end{cases} \tag{10}$$

$$\begin{cases} C_1=\dfrac{2\cdot I_L\cdot V_L\cdot(V_H-V_L)}{\Delta v_{Cp}\cdot f\cdot V_H\cdot({V_H}^2+4\cdot V_L\cdot V_H+3\cdot {V_L}^2)} \\ C_L=\dfrac{2\cdot I_L\cdot(V_H-V_L)}{\Delta v_{Cp}\cdot f\cdot V_H\cdot(V_H+3\cdot V_L)} \\ C_H=\dfrac{\Delta i_{Lp}\cdot I_L\cdot V_L}{8\cdot\Delta v_{Cp}\cdot f\cdot {V_H}^2}\end{cases} \tag{11}$$

Comparisons with other converters

In order to compare the proposed converter with other topologies, three additional metrics are used apart from the conversion ratio: the total inductor energy (12), the total capacitor energy (15), and the total active switch stress (18). The inductor energies are calculated in (13), and the total energy in (14).

$$W_{L_{Tot}}=\sum_{i=1}^{3}\frac{L_i\cdot I_{L_i}^2}{2} \tag{12}$$

$$\begin{cases} W_{L_1} = \dfrac{L_1 \cdot {I_{L_1}}^2}{2} \\ W_{L_3} = \dfrac{L_3 \cdot {I_{L_3}}^2}{2} \end{cases} \Rightarrow \begin{cases} W_{L_1} = \dfrac{I_L \cdot V_L \cdot ({V_H}^2 - {V_L}^2)}{4 \cdot \Delta i_{Lp} \cdot f \cdot V_H \cdot (V_H + 3 \cdot V_L)} \\ W_{L_3} = \dfrac{I_L \cdot {V_L}^2 \cdot (V_H - V_L)}{\Delta i_{Lp} \cdot f \cdot V_H \cdot (V_H + 3 \cdot V_L)} \end{cases} \tag{13}$$

$$W_{L_{Tot}} = 2 \cdot W_{L_1} + W_{L_3} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot \Delta i_{Lp} \cdot f \cdot V_H} \tag{14}$$

The energy from each capacitor is calculated in (16), and the total energy is calculated in (17).

$$W_{C_{Tot}} = \sum_{i=1}^{3} \frac{C_i \cdot V_{C_i}^2}{2} \tag{15}$$

$$\begin{cases} W_{C_1} = \dfrac{C_1 \cdot {V_{C_1}}^2}{2} \\ W_{C_L} = \dfrac{C_L \cdot {V_L}^2}{2} \\ W_{C_H} = \dfrac{C_H \cdot {V_H}^2}{2} \end{cases} \Rightarrow \begin{cases} W_{C_1} = \dfrac{I_L \cdot V_L \cdot ({V_H}^2 - {V_L}^2)}{4 \cdot \Delta v_{Cp} \cdot f \cdot V_H \cdot (V_H + 3 \cdot V_L)} \\ W_{C_L} = \dfrac{I_L \cdot {V_L}^2 \cdot (V_H - V_L)}{\Delta v_{Cp} \cdot f \cdot V_H \cdot (V_H + 3 \cdot V_L)} \\ W_{C_H} = \dfrac{\Delta i_{Lp} \cdot I_L \cdot V_L}{16 \cdot \Delta v_{Cp} \cdot f} \end{cases} \tag{16}$$

$$W_{C_{Tot}} = 2 \cdot W_{C_1} + W_{C_L} + W_{C_H} = \frac{I_L \cdot V_L \cdot (V_H \cdot (8 + \Delta i_{Lp}) - 8 \cdot V_L)}{16 \cdot \Delta v_{Cp} \cdot f \cdot V_H} \tag{17}$$

The total active switch stress is defined in (18), as the sum of the voltage stress multiplied by the current stress for each transistor and it aims to approximate to costs/losses of the switching devices. The voltage and current stress for each transistor are given in (19), and the total active switch stress is calculated in (20).

$$S_{Total} = \sum_{j=1}^{4} V_{S_j} \cdot I_{S_j} \tag{18}$$

$$\begin{cases} V_{S_1} = V_{S_2} = \dfrac{V_{C_1} + V_L}{2} = \dfrac{V_H + 3 \cdot V_L}{4}; \quad I_{S_1} = I_{S_2} = I_{L_1} + I_{L_3} = \dfrac{I_L \cdot (V_H + 3 \cdot V_L)}{2 \cdot V_H} \\ V_{S_3} = V_{S_4} = V_{C_1} + V_L = \dfrac{V_H + 3 \cdot V_L}{2}; \quad I_{S_3} = I_{S_4} = \dfrac{I_{L_1} + I_{L_3}}{2} = \dfrac{I_L \cdot (V_H + 3 \cdot V_L)}{4 \cdot V_H} \end{cases} \tag{19}$$

$$S_{Total} = \frac{I_L \cdot (V_H + 3 \cdot V_L)^2}{2 \cdot V_H} \tag{20}$$

A comparison is made between the proposed BHSISC converter and other converters: the conventional buck/boost converter, a quadratic converter [9], a bidirectional hybrid switched inductor converter (BHSI) [15], and a bidirectional hybrid switched capacitor converter (BHSC) [13]. Firstly, from Fig. 5 it can be seen that the proposed BHSISC converter provides a better conversion gain (ratio), requiring the same energy in the inductors as the conventional, the BHSI and BHSC converters, and less than at least 23% less energy compared to the quadratic converter. Secondly, the transistor stress is reduced compared to both BHSI and BHSC with at least 20% less compared to the quadratic converter, which results in lower losses. Thirdly, the required capacitor energy is also smaller than the required energy for the quadratic converter, but close to the BHSI and BHSC, with the small difference coming from Δi_{Lp}. All the comparisons were made for V_H=400 V and V_L between 20V to 100V voltage levels, which are common to the dc microgrids with supercapacitor storage.

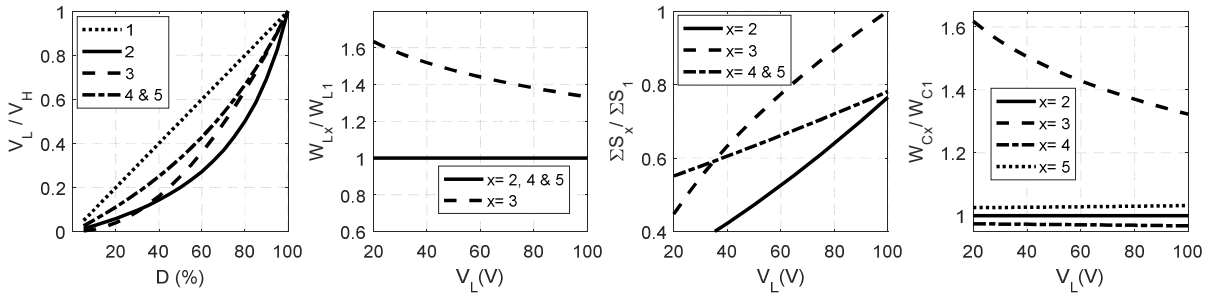

Fig. 5. Comparison of the proposed BHSISC topology with other topologies (1. Conventional Buck/Boost, 2. the BHSISC, 3. Quadratic [9], 4. BHSI [15], 5. BHSC [13])

Stability analysis

Because of the larger number of passive components, the BHSISC is characterized by a higher order system, therefore it is important to analyze its stability prior to the final design, as some instabilities might arise from the hardware design [16].

In order to address the stability, the state space average (SSA) method is used. The parasitic components used for this method are shown in Fig. 6, and the schematics for the two switching states are shown in Fig. 7 and Fig. 8, for t_{on} and t_{off} respectively.

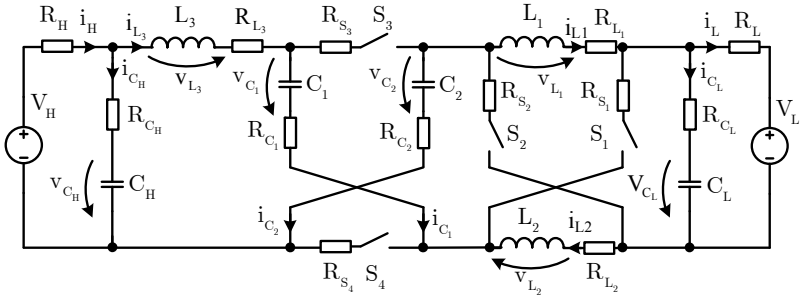

Fig. 6: BHSISC schematic with parasitic components.

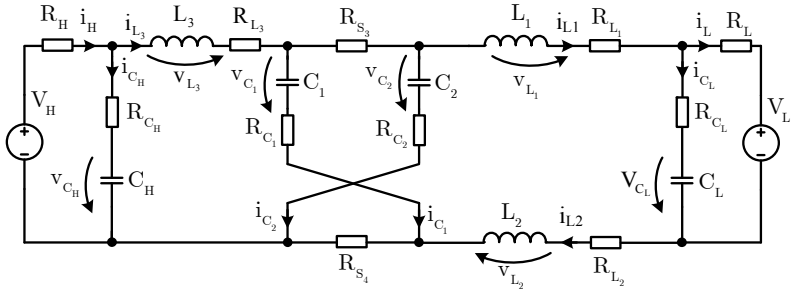

Fig. 7: BHSISC schematic with parasitic components during t_{on}.

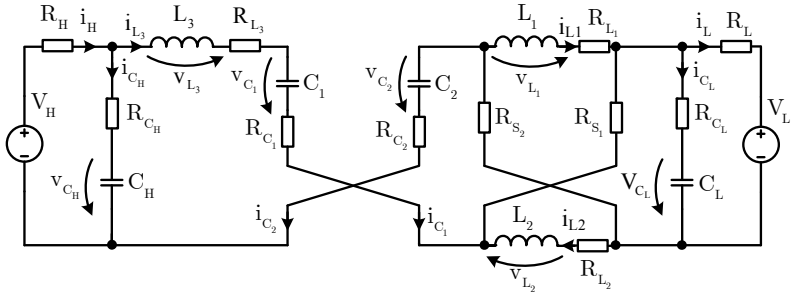

Fig. 8: BHSISC schematic with parasitic components during t_{off}.

Considering a state vector *x*, an input vector *u,* the state space representation for the two equivalent states is written (21) (i=1 for t_{on}, i=2 for t_{off}). The state vector, the input vector and the two matrixes, A_i and B_i, are detailed in (22), and all the elements from the matrixes are expressed from (23) to (34). It is important to mention that for the SSA the following simplifying aspects are made: $i_{L_2} = i_{L_1}$ and $v_{C_2} = v_{C_1}$.

$$\dot{x} = A_i \cdot x + B_i \cdot u \tag{21}$$

$$x = \begin{bmatrix} i_{L_1} \\ i_{L_3} \\ v_{C_1} \\ v_{C_L} \\ v_{C_H} \end{bmatrix}; \quad u = \begin{bmatrix} V_L \\ V_H \end{bmatrix}; \quad A_i = \begin{bmatrix} a_{11_i} & a_{12_i} & a_{13_i} & 0 & a_{15_i} \\ a_{21_i} & a_{22_i} & a_{23_i} & a_{24_i} & a_{25_i} \\ a_{31_i} & a_{32_i} & 0 & 0 & 0 \\ 0 & a_{42_i} & 0 & a_{44_i} & 0 \\ a_{51_i} & a_{52_i} & 0 & 0 & a_{55_i} \end{bmatrix}; \quad B_i = \begin{bmatrix} 0 & b_{12_i} \\ b_{21_i} & b_{22_i} \\ 0 & 0 \\ b_{41_i} & 0 \\ 0 & b_{52_i} \end{bmatrix}; \tag{22}$$

$$a_{11_1} = -\frac{\frac{R_{C_1}}{4} + R_{L_1} + \frac{R_{S_3}}{4} + \frac{R_{C_L} \cdot R_L}{2 \cdot (R_{C_L} + R_L)}}{L_1}; a_{12_1} = \frac{R_{C_1} - R_{S_3}}{4 \cdot L_1}; a_{13_1} = \frac{1}{2 \cdot L_1}; a_{15_1} = -\frac{R_L}{2 \cdot L_1 \cdot (R_{C_L} + R_L)}; \tag{23}$$

$$a_{21_1} = \frac{R_{C_1} - R_{S_3}}{2 \cdot L_3}; a_{22_1} = \frac{\frac{R_{C_1}}{2} + R_{L_3} + \frac{R_{S_3}}{2} + \frac{R_{C_H} \cdot R_H}{R_{C_H} + R_H}}{L_3}; a_{23_1} = -\frac{1}{L_3}; a_{24_1} = \frac{R_H}{L_3 \cdot \left(R_{C_H} + R_H\right)}; a_{25_1} = 0; \tag{24}$$

$$a_{31_1} = -\frac{1}{2 \cdot C_1}; a_{32_1} = \frac{1}{2 \cdot C_1}; a_{42_1} = -\frac{R_H}{C_H \cdot \left(R_{C_H} + R_H\right)}; a_{44_1} = -\frac{1}{C_H \cdot \left(R_{C_H} + R_H\right)}; \tag{25}$$

$$a_{51_1} = \frac{R_L}{C_L \cdot \left(R_{C_L} + R_L\right)}; \quad a_{52_1} = 0; \quad a_{55_1} = -\frac{1}{C_L \cdot \left(R_{C_L} + R_L\right)}; \tag{26}$$

$$b_{12_1} = -\frac{R_{C_L}}{2 \cdot L_1 \cdot (R_{C_L} + R_L)}; b_{21_1} = \frac{R_{C_H}}{L_3 \cdot (R_{C_H} + R_H)}; b_{41_1} = \frac{1}{C_H \cdot (R_{C_H} + R_H)}; b_{52_1} = \frac{1}{C_L \cdot (R_{C_L} + R_L)}; \tag{27}$$

$$a_{11_2} = -\frac{R_{L_1} + R_{S_1} + \frac{2 \cdot R_{C_L} \cdot R_L}{R_{C_L} + R_L}}{L_1}; a_{12_2} = -\frac{R_{S_1} + \frac{R_{C_L} \cdot R_L}{R_{C_L} + R_L}}{L_1}; a_{13_2} = 0; a_{15_2} = -\frac{R_L}{L_1 \cdot (R_{C_L} + R_L)}; \tag{28}$$

$$a_{21_2} = -\frac{2 \cdot R_{S_1} + \frac{2 \cdot R_{C_L} \cdot R_L}{R_{C_L} + R_L}}{L_3}; a_{22_2} = \frac{2 \cdot R_{C_1} + R_{L_3} + 2 \cdot R_{S_1} + \frac{R_{C_H} \cdot R_H}{R_{C_H} + R_H} + \frac{R_{C_L} \cdot R_L}{R_{C_L} + R_L}}{L_3}; \tag{29}$$

$$a_{23_2} = -\frac{2}{L_3}; \quad a_{24_2} = \frac{R_H}{L_3 \cdot (R_{C_H} + R_H)}; \quad a_{25_2} = -\frac{R_L}{L_3 \cdot (R_{C_L} + R_L)}; \quad a_{31_2} = 0; \quad a_{32_2} = \frac{1}{C_1}; \tag{30}$$

$$a_{42_2} = -\frac{R_H}{C_H \cdot (R_{C_H} + R_H)}; \quad a_{44_2} = -\frac{1}{C_H \cdot (R_{C_H} + R_H)}; \tag{31}$$

$$a_{51_2} = \frac{2 \cdot R_L}{C_L \cdot (R_{C_L} + R_L)}; \quad a_{52_2} = \frac{R_L}{C_L \cdot (R_{C_L} + R_L)}; \quad a_{55_2} = -\frac{1}{C_L \cdot (R_{C_L} + R_L)}; \tag{32}$$

$$b_{12_2} = -\frac{R_{C_L}}{L_1 \cdot (R_{C_L} + R_L)}; \quad b_{21_2} = \frac{R_{C_H}}{L_3 \cdot (R_{C_H} + R_H)}; \quad b_{22_2} = -\frac{R_{C_L}}{L_3 \cdot (R_{C_L} + R_L)}; \tag{33}$$

$$b_{41_2} = \frac{1}{C_H \cdot (R_{C_H} + R_H)}; \quad b_{52_2} = \frac{1}{C_L \cdot (R_{C_L} + R_L)}; \tag{34}$$

If a variable duty cycle is considered (*d*), the averaged model can be described with (35). If the system is linearized around a steady state duty cycle, *D*, for a small signal variation, $\tilde{d}$ (with $d = D + \tilde{d}$), the system can be obtained in (36), with the equivalent matrixes described in (37). The transfer functions which are of interest, (38), are obtained from (39), by setting C_e=[1 0 0 0 0] or C_e=[0 1 0 0 0] respectively.

$$\dot{x} = (A_1 \cdot d + A_2 \cdot (1-d)) \cdot x + (B_1 \cdot d + B_2 \cdot (1-d)) \cdot u \tag{35}$$

$$\begin{cases} \dot{\tilde{x}} = A_e \cdot \tilde{x} + B_e \cdot \tilde{d} \\ \tilde{y} = C_e \cdot \tilde{x} \end{cases} \tag{36}$$

$$\begin{aligned} A_e &= (A_1 \cdot D + A_2 \cdot (1-D)) \\ B_e &= [(A_1 - A_2) \cdot X + (B_1 - B_2) \cdot u] \end{aligned} \tag{37}$$

$$H_1(s) = \frac{\tilde{i}_{L_1}(s)}{\tilde{d}(s)}; \quad H_2(s) = \frac{\tilde{i}_{L_3}(s)}{\tilde{d}(s)}; \tag{38}$$

$$\tilde{y} = C_e \cdot (s \cdot I - A_e)^{-1} \cdot B_e \cdot \tilde{d} \tag{39}$$

In order to analyze the stability, a preliminary selection of components is necessary, therefore, the parameters from Table I are calculated using (5), (8) and (11). Starting with Table I, the components from Table II are selected, as well as transistors with resistances of 15mΩ and 50mΩ for S1/S2 and S3/S4 respectively.

Even if the theoretically required capacitance is small in selected values, where film or ceramic capacitors can be used, they might introduce right-half-plane zeros (RHPZ) due to low ESR [16]. An RHPZ can be observed in Table III, where the poles and zeros of the system are provided. The results are calculated using the capacitors from Table I with an equivalent ESR of 1mΩ (R_{C_L} & R_{C_1}) and 3mΩ (R_{C_H}), and the rest of the components from Table II. The poles and zeros for the system with the electrolytic capacitors from Table II are shown in Table IV, proving that the RHPZ disappears in this case. Even if (11) might not be sufficient for choosing the capacitors, it still is useful for comparing to other topologies.

Table I: Initial design values.

Element	V_H	V_L	I_L	f_{sw}	Δi_{Lp}	Δv_{Cp}	L_1, L_2	L_3	C_1, C_2	C_L	C_H	D
Value	400	50	80	80	20	2	44.19	398	17.6	159	0.39	37.21
Unit	V	V	A	kHz	%	%	µH	µH	µF	µF	µF	%

Table II: Final design values.

Element	L_1, L_2	R_{L_1},R_{L_2}	L_3	R_{L_3}	C_1, C_2	R_{C_1},R_{C_2}	C_L	R_{C_L}	C_H	R_{C_H}
Value	47	4	470	53	4x 1.2	95 /4	7x 6.8	15/7	680	160
Unit	µH	mΩ	µH	mΩ	mF	mΩ	mF	mΩ	µF	mΩ
Component	DEMS-55/0.047/60-S		DEHF-42/0.47/16 DLA		4x MAL2 259 73122 E3		7x. MAL2 256 58682 E3		1x MAL2 095 76681 E3	

Table III: Poles and zeros for the initial design.

Transfer function	**Poles**	**Zeros**
$H_1(s)$	-4.2735e+8; -3.1446e+6; -479.8670; -5.9596e+1 ± 1.4213e+4i;	-4.2735e+8; -3.1452e+06; **1.1181e+3 ± 1.3946e+4i;**
$H_2(s)$	-4.2735e+8; -3.1446e+6; -479.8670; -5.9596e+1 ± 1.4213e+4i;	-4.2735e+8; -3.1449e+6; -5.2108e+3 ± 1.4239e+4i

Table IV: Poles and zeros of the final design.

Transfer function	Poles	Zeros
$H_1(s)$	-4.8678e+3; -4.4046e+3; -636.2373 -2.3513e+2 ± 8.3529e+2i;	-4.9048e+3; -4.4104e+3; -2.694e+2 ± 8.1917e+2i
$H_2(s)$	-4.8678e+3; -4.4046e+3; -636.2373; -2.3513e+2 ± 8.3529e+2i;	-4.8842e+3; -4.5956e+3; -1.2825e+2 ± 9.1384e+2i;

The bi-directional feature of the BHSISC requires a current controller; therefore, the L_1 inductor current is used for control as its transfer function has a higher gain. The controller is chosen based on the linearized SSA model which is in good correspondence to the small signal frequency response obtained by simulation (Fig. 9 - left). In order to obtain a phase margin (PM) of 85° at the crossover frequency (f_c) of 20kHz, the controller with the transfer function from (40) is implemented, obtaining the open-loop frequency response from Fig. 9 - right. The simulation results from Fig. 10, also confirm the stability of the converter and a fast transition between the two operating modes, with small overshoot on L_1 inductor current. Small damped oscillations are present in the L_3 inductor current, so a low-pass filter can be used for the reference value, as it was applied in [13].

$$C(s) = \frac{0.042814 \cdot (s + 1.478 \cdot 10^4)}{s} \tag{40}$$

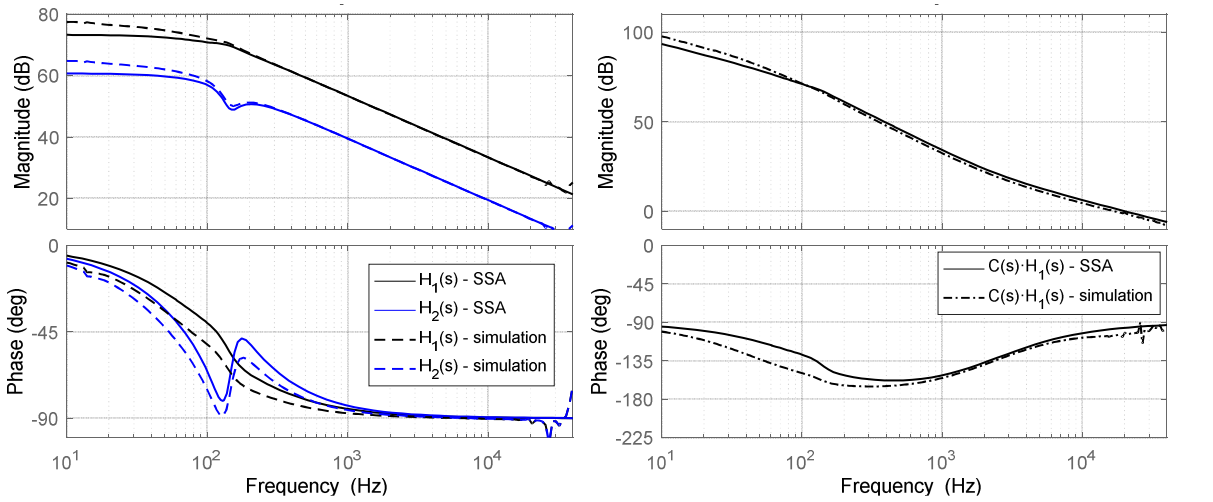

Fig. 9: BHSISC Bode diagrams: left - $H_1(s)$ and $H_2(s)$ response; right - $C(s)\cdot H_1(s)$ open loop response with controller (PM=85°; f_c=80kHz).

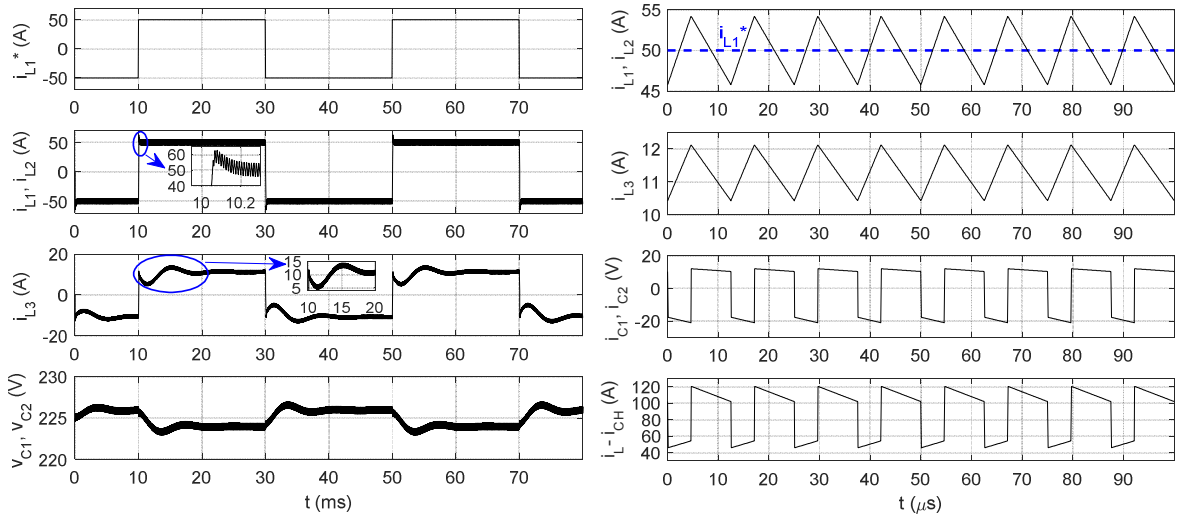

Fig. 10: Simulation results: I_{L_1} =±50A (transient - Left), 50A (steady state - right), V_H=400V, V_L=50V.

Conclusion

This paper proposes a new converter topology, offering analytical descriptions and simulation results. The advantages of the proposed topology have been presented, including the high conversion ratio, advantages in inductor size, capacitor size, and the active switches stress reduction. All these factors were used as metrics for the topology and performance comparison with other related topologies. The simulation results of the topology and its controller design demonstrated a stable and robust operation. The fast transitions between the two operating regimes, buck and boost, have been successfully achieved. The control and stability of the topology were addressed, with emphasis on passive components selection and overall converter design.

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